Introduction to Digital Logic

EECS/CSE 31L

**Assignment 4 Design Report**

**Designing Counter**

prepared by: Derek Yang

Student ID: 63118832

EECS Department

Henry Samueli School of Engineering

University of California, Irvine

November, 8, 2014

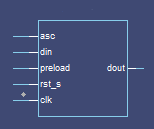
1 BLOCK Description

This 32bit counter takes a 32bit input and counts up or down depending on the ascending mode given, 0 meaning decrement and 1 meaning increment. This counter circuit is also synchronous, meaning it will rely on the clock cycle to take action, so only when the clock is 1, the counter will increment or decrement. The preload mode also enables the user to load their input into the counter. There is also a reset mode, where when enabled, all inputs and counts will return to 0.

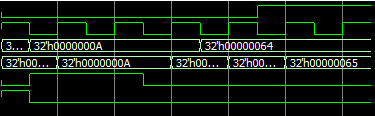
2 Input/Output Port Description

|  |  |  |  |
| --- | --- | --- | --- |
| Port Name | Port Size | Port Type | Description |
| clk | 1 | IN | The Clock Cycle |
| rst\_s | 1 | IN | Synchronous Reset Signal (1 = Reset) |
| asc | 1 | IN | Ascending Signal (0 = Decrement, 1 = Increment) |
| preload | 1 | IN | Mode Selection (0=Arithmetic, 1=Logical) |
| din | 32 | IN | 32-bit Input |
| dout | 32 | OUT | 32-bit Output |

3 Design Schematic



4 Wave



asc

clk

din

dout

preload

rst\_s